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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,707	11/03/2003	Antonio F. Mondragon-Torres	TI-35731	3525

23494 7590 03/20/2007

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
LEE, SIU M	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,707	MONDRAGON-TORRES ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/3/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,16,17,19,20 and 22* is/are rejected.

7)☒ Claim(s) *11-15,18 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Paragraph 0044, line 4 recites the "delay line 212". According to figure 2d, the reference number of delay line is 512.

Appropriate correction is required.

Drawings

2. The drawings are objected to because figure 3 does not show the system number 300 as reference in paragraph 0045, lines 2 and 3, also figure 4 does not show the system number 400 as reference in paragraph 0046, lines 2 and 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application

must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 17 is objected to because of the following informalities:

Line 7 of claim 17 recites "the signal profile". There is no antecedent basis for the signal profile.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 3, 4, 6, 10, 16, 17, 19, 20, 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueda (US 5,644,597).

(1) Regarding claim 1:

Ueda discloses an apparatus comprising:

two or more adaptive equalizers (adaptive equalizer 175, 176,180 and 181 in figure 14);

a plurality of operational blocks that interconnect the adaptive equalizers (received-signal memory 110 and 117 and delay measurement circuit 174, 179, square error integrated circuit 177, 182, equalized-output memory 178, 183 and selecting circuit 185 in figure 14); and

a control mechanism that configures the adaptive equalizers and operational blocks according to different signal delay profiles (delay measurement circuit 174 and 179 in figure 14, the delay measurement circuit 174 outputs a control signal that make a decision as to whether either one of the decision feedback adaptive equalizer 175 and the linear adaptive equalizer 176 should be operated with respect to its burst depending on the ratio of the value of the direct wave of the correlator to that of the delay wave thereof and the maximum delay time of the delay wave, same apply to the delay measuring circuit 179, column 46, lines 51-63).

(2) Regarding claim 2:

Ueda further disclose a second control mechanism that disables at least one of said plurality of operational blocks according to the different signal delay profiles (the comparator outputs the result of selector to the selecting circuit and outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, column 36, lines 13-19).

(3) Regarding claim 3:

Ueda further discloses wherein each of said two or more adaptive equalizers comprise a computational resource (the decision feedback adaptive equalizer 175, 180 and linear adaptive equalizers 176, 181 read data from the received-signal memory 110

and 117 and estimate characteristics of a channel using UW11 as described in the paragraph of the operation of the equalizer shown in fig. 15, column 47, lines 11-30 and column 1, lines 40-67).

(4) Regarding claim 4:

Ueda further discloses wherein the computation resource comprises at least one item selected from the group consisting of a summer, a conjugation block, a multiplier, and a divider (with respect to figure 15, there are adder 3 and 5, column 1, lines 40-67).

(5) Regarding claim 6:

Ueda discloses wherein said operational blocks comprise at least one item selected from the group consisting of: a signal regenerator; a delay line; and a summer (among the operational block listed in claim 1, the delay measuring circuit 174 and 179 contains a correlator to correlate the unique word (UW) with the received signal, it is inherent that a correlator would comprise a summer, column 46, lines 51-54).

(6) Regarding claim 10:

Ueda discloses receiving a multi-path signal profile (abstract, lines 2-4); determining attributes of the multi-path signal profile (a plurality of delay measuring circuits each supplied with each detected signal as input and for detecting a multipath propagation characteristics of a channel, column 14, lines 47-50); and operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and operational blocks interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile (means for selecting one of the equalized outputs produced from the plurality of decision feedback adaptive

equalizers or one of equalized outputs produced from the plurality of linear adaptive equalizers based on the results measured by the delay measuring circuits and setting the selected one equalized output as a final equalized output, whereby the adaptive equalizers which are expected to show better performance than that of the other with respect to the multipath propagation characteristics measured by the respective delay measuring circuits, are activated every branches to thereby produce equalized outputs for every branches and characteristics of the equalized outputs produced every branches are thereafter compared to thereby set the output of the adaptive equalizer which is best in equalization characteristic as a final equalized output from the result of comparison, column 14, lines 50-65).

(7) Regarding claim 16:

Ueda further discloses that disabling at least one selected from the group: adaptive equalizer; operational block; and computational resource (the performance of the plurality of decision feedback adaptive equalizers and those of the plurality of linear adaptive equalizers are respectively compared to thereby set the output of one of the adaptive equalizers, which is best in equalization characteristic, as a final equalized output from the result of comparison, and the remaining adaptive equalizers are deactivated, column 12, lines 41-48).

(8) Regarding claim 17 (the examiner interpreted "the signal profile" as "a signal profile" in line 7 of claim 17):

Ueda discloses a system comprising two or more adaptive equalizers (adaptive equalizer 127, 130,133, 136 in figure 11); a plurality of operational blocks (received-

signal memory 110 and 117 and square error integrated circuits 128, 131, 134, 137, equalized-output memory 129, 132, 135, 138 and comparator 139, and selecting circuit 140 in figure 11); means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks (the comparator 139 compares the results outputted from the equalized square error integrating circuit 128, the equalized square error integrating circuit 131, the equalized square error integrating circuit 134 and the equalized square error integrating circuit 137. Next, the comparator 139 selects the adaptive equalizer which is expected to have the minimum sum of equalized square errors, i.e., to have the best performance with respect to its burst. Thereafter, the comparator 139 outputs the result of selection to the selecting circuit 140 and outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected. These adaptive equalizers stop the equalization of the remaining random data corresponding to the same burst in response to the stop signal, column 36, lines 6-19); and means for configuring the two or more adaptive equalizers and operational blocks according to attributes of the signal profile (the decision feedback adaptive equalizer which shows excellent performance under frequency selective fading in which a delay time interval of a delay wave is long and the linear adaptive equalizer which shows excellent performance under frequency selective fading in which a delay time interval of a delay wave is short and fading in which a delay wave does not exist, therefore, when the comparator 139 compares the square error of each adaptive equalizer, it is comparing according to the signal profile of the incoming signal and from the

comparison, decide which adaptive equalizer to use and which adaptive equalizer to deactivate, column 15, lines 16-23).

(9) Regarding claim 19:

Ueda discloses the system comprises means for disabling at least one of the plurality of operational blocks according to said attributes of the signal profile (the comparator 139 outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, column 36, lines 13-17).

(10) Regarding claim 20:

Ueda discloses the system comprises means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile (the comparator 139 outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, column 36, lines 13-17).

(11) Regarding claim 22:

Ueda discloses the system wherein the attributes of the signal profile comprise at least one selected from the group consisting of: a number of antennas that transmitted the multi-path signal; a length of the multi-path signal profile; an amount of energy in a single sub-signal of the multi-path signal; an amount of capturable energy by a number of adaptive equalizers; and a number of energy clusters (Ueda discloses the attributes of the signal profile comprises a length of the multi-path signal profile, there is a method of activating the linear adaptive equalizer 176 if the maximum delay time of the delay wave is less than or equal to 0.35 symbol and of activating the decision feedback

adaptive equalizer 175 if the maximum delay time is more than or equal to 0.35 symbol, column 46, line64 – column 47, line 2).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Liang et al. (US 2003/0133424 A1).

(1) Regarding claim 1:

Liang et al. discloses an apparatus comprising:

two or more adaptive equalizers (a plurality of adaptive equalizers 508A – 508C in figure 5, paragraph 0074, lines 3-5);

a plurality of operational blocks that interconnect the adaptive equalizers (the cell searcher 502 processes the input, and is connected and provides input to the code generator 504, the code generator 504 processes the input and in turn is connected and provides input to the power delay profile estimator 503, multiple short equalizers (SE) 508 and multiple time-alignment and despreader modules (TADs) 510, the power delay profile estimator 503 processes all inputs and is connected and provides input to the

intelligent cluster analyzer 505, which in turn process all inputs and is connected and provides input to the multiple SEs 508 and multiple TADs 510 paragraph 0074); and

a control mechanism that configures the adaptive equalizers and operational blocks according to different signal delay profiles (as discloses in fig. 10-12, with reference to different power delay profiles (hilly terrain, typical urban, equalization test), the intelligent cluster analyzer 505 generates information regarding the number of SEs 508, and the filter length and the reference timing of the SEs 508, paragraph 0094, lines 1-6).

(2) Regarding claim 7:

Liang et al. discloses wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of: sub-signals that arrive to the apparatus in consecutive chip time units; sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals; sub-signals that do not arrive to the apparatus in consecutive chip time units; sub-signals that arrive to the apparatus in two or more clusters; sub-signals that arrive to the apparatus from more than one antenna (with respect to figure 10, the hilly terrain power delay profile model, with respect to figure 11, the typical urban power-delay profile model, with respect to figure 12, the equalization test power-delay profile model, paragraph 0095, 0100, and 0103).

(3) Regarding claim 10:

Liang et al discloses a method comprising:

receiving a multi-path signal profile (paragraph 0039, liens 5-9, claim 9 in page 12);

determining attributes of the multi-path signal profile (different power delay profile as discloses in fig. 10-12, the intelligent cluster analyzer 505 generates information regarding the number of SEs 508, and the filter length and the reference timing of the SEs 508, paragraph 0094, lines 1-6); and

operating two or more adaptive equalizers (508A – 508C in figure 5), computational resources of the two or more adaptive equalizers, and operational blocks interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile (the intelligent cluster analyzer 505, which in turn process all inputs and is connected and provides input to the multiple SEs 508 and multiple TADs 510 paragraph 0074, lines 16-20, the intelligent cluster analyzer 505 generates information regarding the number of SEs 508, and the filter length and the reference timing of the SEs 508, paragraph 0094, lines 1-6, paragraph 0075, lines 21-30).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Yang (US 6,763,074 B1).

Ueda discloses all the subject matter as discuss in claim 1 except wherein a two-stage configuration of the apparatus comprises a default mode.

However, Yang discloses wherein a two-stage configuration of the apparatus comprises a default mode (step 1600 in figure 16, the default mode is selected from a plurality of possible modes of operation, column 10, lines 17-20).

It is desirable wherein a two-stage configuration of the apparatus comprises a default mode because at least the output of a detector appears at the output of the multiplexor and if the same detector is selected, the system can continue with the preselected default detector (column 1, line 65 – column 2, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Yang in the system of Ueda to provide a more efficient system.

Double Patenting

10. Claims 1-8, 17, 19, 20, 22 are provisionally rejected on the ground of nonstatutory double patenting over claims 1-8, 18-21 of copending Application No. 11/105,755. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

(1) Regarding claim 1, the same matter is claimed in claim 1 of the application 11/105,755.

(2) Regarding claim 2, the same matter is claimed in claim 2 of the application 11/105,755.

(3) Regarding claim 3, the same matter is claimed in claim 5 of the application 11/105,755.

(4) Regarding claim 4, the same matter is claimed in claim 6 of the application 11/105,755.

(5) Regarding claim 5, the same matter is claimed in claim 3 of the application 11/105,755.

(6) Regarding claim 6, the same matter is claimed in claim 7 of the application 11/105,755.

(7) Regarding claim 7, the same matter is claimed in claim 8 of the application 11/105,755.

(8) Regarding claim 8, the same matter is claimed in claim 4 of the application 11/105,755.

(9) Regarding claim 17, the same matter is claimed in claim 18 of the application 11/105,755.

(10) Regarding claim 19, the same matter is claimed in claim 19 of the application 11/105,755.

(11) Regarding claim 20, the same matter is claimed in claim 20 of the application 11/105,755.

(12) Regarding claim 22, the same matter is claimed in claim 21 of the application 11/105,755.

The chart below summarizes the double patenting issues.

Claims	Current application 10/699,707	11/105,755	Claim
1	An apparatus comprising: two or more adaptive equalizers; a plurality of operational blocks that interconnect the adaptive equalizers; and a control mechanism that configures the adaptive equalizers and operational blocks according to different signal delay profiles.	A system, comprising: a plurality of adaptive equalizers adapted to couple to a plurality of receive antennas, each of said antennas capable of receiving a multipath delay profile estimate (MDPE); control logic interconnecting at least some of the adaptive equalizers; and a control mechanism that, according to different MDPEs, configures at least some of the adaptive equalizers and circuit control logic.	1
2	The apparatus of claim 1 further comprising a second control mechanism that disables at least	The system of claim 1, further comprising a second control mechanism that disables at least	2

	one of said plurality of operational blocks according to the different signal delay profiles.	a portion of said control logic according to the different MDPEs.	
3	The apparatus of claim 2 wherein each of said two or more adaptive equalizers comprise a computational resource.	The system of claim 1, wherein at least one of the adaptive equalizers comprises a computational resource.	5
4	The apparatus of claim 3 wherein the computation resource comprises at least one item selected from the group consisting of a summer, a conjugation block, a multiplier, and a divider.	The system of claim 5, wherein the computation resource comprises at least one item selected from the group consisting of a summer, a conjugation block, a multiplier and a divider.	6
5	The apparatus of claim 2 further comprising a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different signal delay profiles.	The system of claim 2, further comprising a third control mechanism that disables a computation resource of at least one of said adaptive equalizers according to the different MDPEs.	3
6	The apparatus of claim 1 wherein	The system of claim 1, wherein	7

	said operational blocks comprise at least one item selected from the group consisting of: a signal regenerator; a delay line; and a summer.	said control logic comprises at least one item selected from the group consisting of: a signal regenerator; a delay line; and a summer.	
7	The apparatus of claim 1 wherein the different signal delay profiles comprise at least one multi-path signal profile selected from the group consisting of: sub-signals that arrive to the apparatus in consecutive chip time units; sub-signals wherein one sub-signal comprises a substantial amount of total energy of the sub-signals; sub-signals that do not arrive to the apparatus in consecutive chip time units; sub-signals that arrive to the apparatus in two or more clusters; sub-signals that arrive to the apparatus from more than one antenna.	The system of claim 1, wherein the different multipath delay profile estimates (MDPEs) comprise at least one MDPE selected from the group consisting of: sub-signals, at least some of which arrive to the system in consecutive chip time units; sub-signals, at least one of which comprises a substantial amount of total energy of the sub-signals; sub-signals that do not all arrive to the system in consecutive chip time units; sub-signals, at least some of which arrive to the system in two or more clusters; sub-signals, at	8

		least some of which arrive to the system by way of more than one receive antenna; and sub-signals, at least some of which arrive to the system in groups of two or more.	
8	The apparatus of claim 5 wherein the first, second, and third control mechanisms comprise multiplexers that receive control signals according to the different signal delay profiles.	The system of claim 3, wherein the first, second and third control mechanisms comprise multiplexers that receive control signals according to the different MDPEs.	4
17	A system comprising: two or more adaptive equalizers; a plurality of operational blocks; means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks; and means for configuring the two or more adaptive equalizers and operational blocks according to attributes of the	A system, comprising: at least two receive antennas, each antenna capable of receiving a multipath delay profile estimate (MDPE); at least two adaptive equalizers coupled to said receive antennas; control logic coupled to the at least two adaptive equalizers; means for selectively interconnecting the at least two	18

	signal profile.	adaptive equalizers and the control logic; and means for configuring the at least two adaptive equalizers and control logic according to attributes of at least one MDPE.	
19	The system of claim 17 further comprising means for disabling at least one of the plurality of operational blocks according to said attributes of the signal profile.	The system of claim 18, further comprising means for disabling at least a portion of the control logic.	19
20	The system of claim 17 further comprising means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said attributes of the signal profile.	The system of claim 18, further comprising means for disabling a computational resource of at least one of the adaptive equalizers.	20
22	The system of claim 17, wherein the attributes of the signal profile comprise at least one selected from the group consisting of: a	The system of claim 18, wherein the attributes of the MDPE comprise at least one selected from the group consisting of: a	21

	number of antennas that transmitted the multi-path signal; a length of the multi-path signal profile; an amount of energy in a single sub-signal of the multi-path signal; an amount of capturable energy by a number of adaptive equalizers; and a number of energy clusters.	number of antennas that transmit the multipath signal; a number of antennas that receive the multipath signal; a length of the MDPE; an amount of energy in a single sub-signal of the multipath signal; an amount of capturable energy by a number of adaptive equalizers; and a number of energy clusters.	

Allowable Subject Matter

11. Claims 11-15, 18, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Juan (US 5,642,382) discloses a FIR filters with multiplexed inputs suitable for use in reconfigurable adaptive equalizers. Smee et al. (US 7,027,503 B2) discloses a receiver with decision feedback equalizer and linear equalizer. Korn (US 5,670,916) discloses adaptive equalizer circuit including multiple equalizer units.

Potter (4,811,360) discloses apparatus and methods for adaptively optimizing equalization delay of data communication equipment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee

3/7/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER